

# Spacecraft Optical Disk Recorder

## Memory Buffer Control

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### I. Project Goals

The goal of this project is to develop an Application Specific Integrated Circuit (ASIC) for use in the control electronics of the Spacecraft Optical Disk Recorder (SODR). Specifically, this project is to design an extendable memory buffer controller ASIC for rate matching between a system Input/Output port and the SODR's device interface.

The aforementioned goal can be partitioned into the following sub-goals:

- 1) Completion of ASIC design and simulation (on-going via ASEE fellowship),
- 2) ASIC Fabrication (@ ASIC manufacturer),
- 3) ASIC Testing (NASA/LaRC, CNU).

### II. Project Description

My research activities during my NASA-ASEE fellowship have been part of the SODR project in the Flight Electronics Division. The SODR project will develop a space qualified optical disk storage system for mass storage and high data rate applications. The system architecture calls for a reconfigurable and extendable optical disk storage system. A multiport system will support terabit capacity and gigabit transfer rates. The disk drive (two devices) requirements call for 10 Gbytes of disk capacity and sustained data rates of 300 Mbps. The high level SODR system architecture is shown in Figure 1.

The specific system being developed in this project is the Memory Buffer Controller (MBC). The function of the MBC is to interface a system I/O port to a SODR device (note each optical disk drive is two devices). Since the instantaneous data rates of the I/O port and the SODR device may vary, a buffer memory is required for data rate matching between these two interfaces.

The current MBC system design calls for an 8-bit data path which is cascadable to support a 32-bit HPPI (High Performance Parallel Interface) data I/O port. The HPPI data port (or multiple HPPI data ports) will be the data I/O path for the SODR system. The MCB's SODR device interface is currently designed to support SCSI II protocol (16-bit, fast). Both interfaces selected have ANSI standards and support the high data rates specified by the SODR system requirements.

Functionally, the MBC ASIC decomposes into the following sections:

- 1) The HPPI source and destination interface,
- 2) The SCSI II interface to the optical disk recorder,
- 3) The Group Controller interface for MBC control and testing,
- 4) The memory buffer interface,
- 5) The MBC system controller.

Figure 2 shows the MBC ASIC with all the major interfaces in a 32-bit I/O port configuration.

### **III. NASA-ASEE Summer Research Activities**

Research activities include:

- 1) System architecture development,
- 2) Interface definitions,
- 3) Memory subsystem design & simulation,
- 4) Control algorithm development.

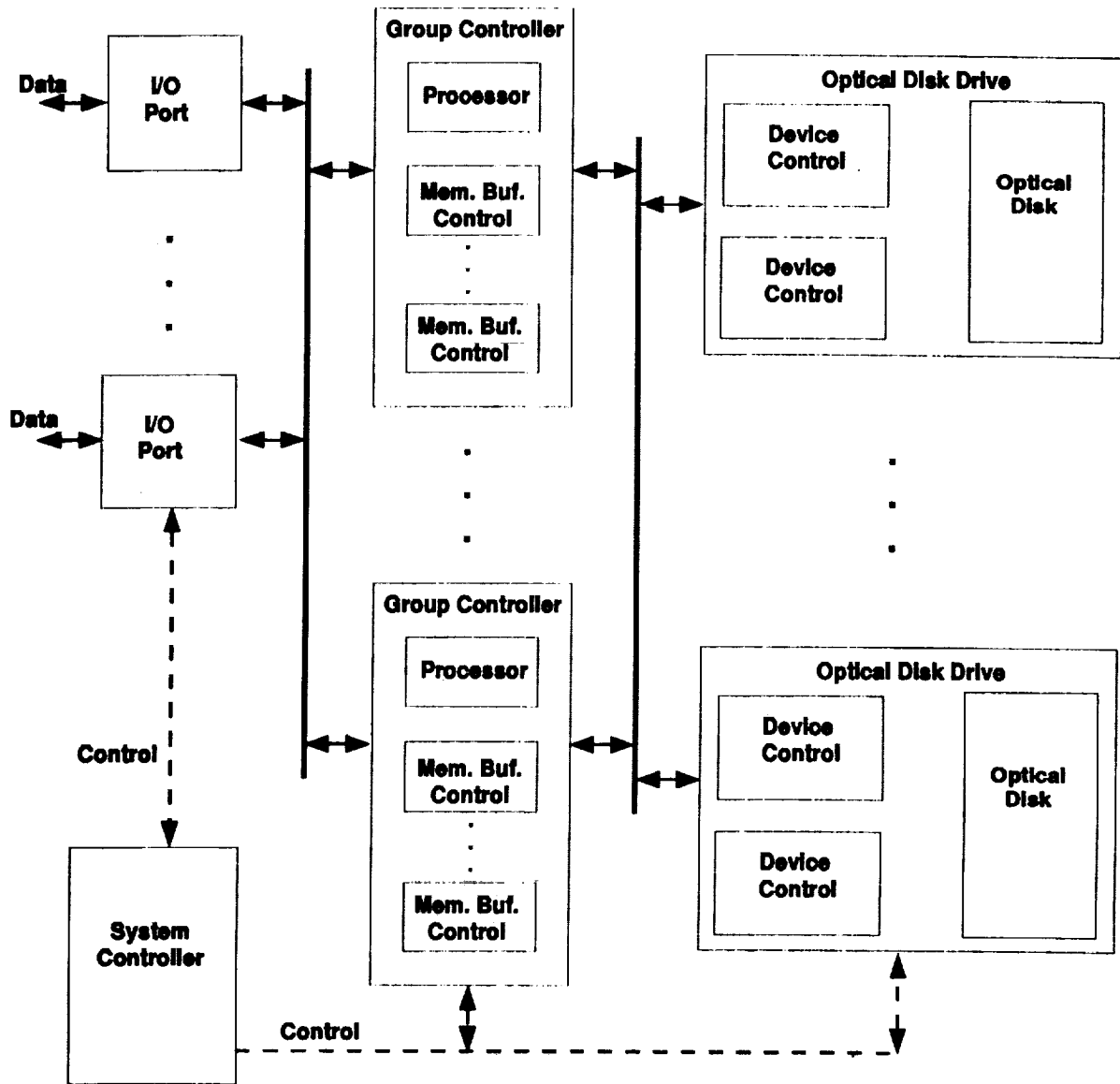
Various system architectures were studied for ASIC implementation. Factors such as device pinout and gate count were considered in determining the final architecture. Interface definitions were determined for both internal subsystems and external ASIC signals. The detailed design of the memory subsystem was completed along with a simulation of this subsystem to verify the subsystem timing. Furthermore, system control algorithms were developed to control data flow and synchronization through the memory buffer and its associated interfaces.

### **IV. ASEE Related Issues**

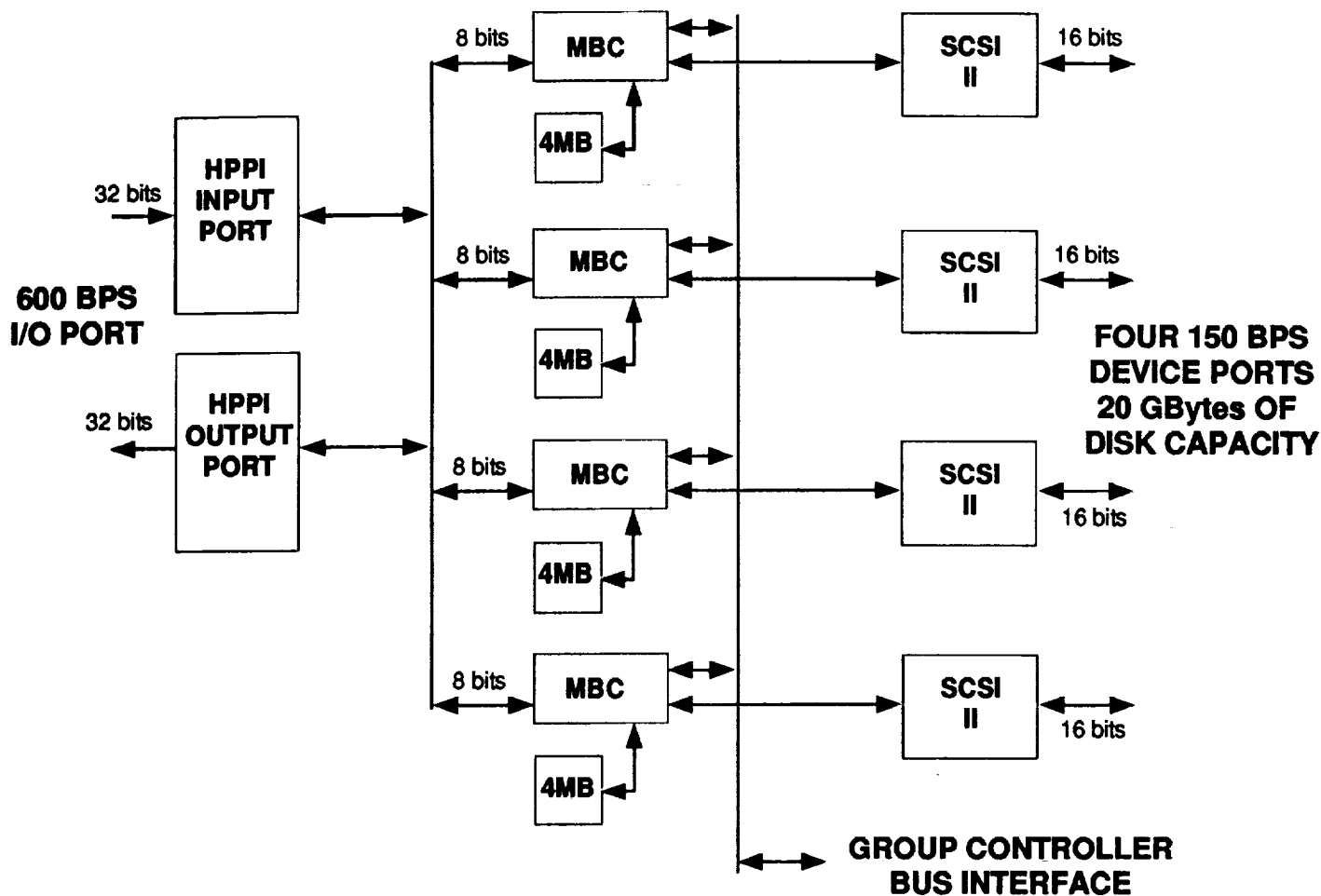
In addition to my research activities, I had the opportunity to use a powerful set of design tools for ASIC development. The use of these tools will extend to the classroom for both undergraduate and graduate courses. Contacts made during my NASA-ASEE fellowship have, in-part, made it possible to bring these tool into a university environment.

### **V. Acknowledgments**

Special thanks to my associate, Steve Jurczyk, and other members of the SODR team for their help and encouragement.



**Figure 1. SODR System Architecture**



**Figure 2. MBC with 32-bit HPPI and 16-bit SCSI**